IDW

Customer No. 22,852
Attorney Docket No.: **04329.3150**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Notice of Allowance: 06/30/04
Mie MATSUO et al.	)	Confirmation No.: **1263**
Application No.: **10/673,192**	)	Group Art Unit: **2815**
Filed: **September 30, 2003**	)	Examiner: **Sheila V. Clark**
For: **STACKED TYPE SEMICONDUCTOR DEVICE**	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUMMARY OF TELEPHONE INTERVIEW

Pursuant to 37 C.F.R. § 1.133 and M.P.E.P. Section 713.04, Applicants' undersigned representative provides the following summary of a telephone interview with Examiner Clark on August 16, 2004.

Applicants' undersigned representative contacted Examiner Clark on August 16 regarding the form PTO-1449 returned by the Examiner as an attachment to the Notice of Allowability dated June 30, 2004. That form PTO-1449 (copy attached) had been previously submitted to the Office as part of an IDS filed with the above referenced application on September 30, 2003. As seen on the attached form PTO-1449, while Examiner Clark signed her initials adjacent the listed U.S. and foreign patent documents, she lined through listed copending U.S. application 09/669,724.

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The specific purpose of Applicants' undersigned representative contacting the Examiner was to ask whether the Examiner has considered copending application 09/669,724 and why she had lined through its listing. Examiner Clark explained that she had considered copending application 09/669,724. However, since the documents listed on the form PTO 1449 will be listed on the face of the issued patent and based on Examiner Clark's understanding that the copending application does not fall into any category of document that can be listed on the face of issued patent, she lined through the listing of the copending application.

Please grant any extensions of time required to enter this paper and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: August 17, 2004

By: _____
Richard V. Burgujian
Reg. No. 31,744

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3150	Serial No.	Not Yet Assigned 10/673192
Applicants	Mie MATSUO et al.		
Filing Date	September 30, 2003	Group:	Not Yet Assigned 2818

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,624,506 B2	09/23/03	SASAKI et al.			
		6,614,106 B2	09/02/03	MATSUO et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2002-110865	04/12/02	JAPAN			ABSTRACT
		2001-102479	04/13/01	JAPAN			ABSTRACT
		2760188	03/20/98	JAPAN			ABSTRACT
		2000-349229	12/15/00	JAPAN			ABSTRACT
		05-283606	10/29/93	JAPAN			ABSTRACT

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	YODA, T. et al., "Semiconductor Integrated Circuit Device Having Interposer And Method of Manufacturing The Same", U.S. Patent Application No. 09/669,724, filed on September 26, 2000.

Examiner	Date Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO 1449 — Patent and Trademark Office - U.S. Department of Commerce